Amendments to the Specification

1. (previously presented) A field effect transistor for detecting a magnetic field comprising:

a doped layer;

doped source and drain regions formed in said doped layer, said doped layer defining a lengthwise extending channel between said source and drain regions;

first and second drain contacts spaced laterally relative to the length of said channel located laterally proximate first and second lateral regions of said channel, respectively, and interconnected with said drain region;

a gate proximate said channel, for controlling current that may flow from said source to said drain region; and

first and second supplemental gates, electrically isolated from each other and said gate and located laterally proximate said first and second lateral regions and said channel, respectively,

wherein said first supplemental gate is interconnected with said second drain contact, and said second supplemental gate is interconnected with said first drain contact, so that said first and second supplemental gates exert a lateral electric field in said channel as a result of imbalanced current flow through said first and second drain contacts.

2. (cancelled)

3. (previously presented) The device of claim 1, wherein said doped layer is formed of p-type semiconductor material, and said source and drain regions are formed of n-type semiconductor material.

4. (previously presented) The device of claim 1, wherein said doped layer is formed of n-type semiconductor material, and said source and drain regions are formed of p-type semiconductor material.

5-8. (canceled)

9. (previously presented)A field effect transistor comprising:
a semiconductor substrate;
a source region and a drain region;
a channel formed in said substrate for guiding current from said source region to said drain region along a lengthwise extent of said channel;
a gate in proximity with said channel for controlling current from said source to said drain;
said drain region comprising first and second drain contacts, each of said first and second drain contacts for guiding current from a lateral portion of said channel;
first and second supplemental gates proximate said channel for establishing an electric field in said channel, in a direction perpendicular to said lengthwise extent;
wherein said first drain contact and said first supplemental gate are located proximate a first lateral region of said channel, and said second drain contact and said second supplemental gate are located proximate a second lateral region of said channel, and said first supplemental gate is electrically interconnected with said second drain contact, and second supplemental gate is electrically interconnected with said first drain contact.

10. (canceled)

11. (cancelled)

12. (currently amended) [[A]] The magnetic latch of claim [[9]] 14, wherein said source and said first drain contact are interconnected to an electronic circuit, to switch current through said first drain contact to said electronic circuit in the presence of a magnetic field.

13. (currently amended) A magnetic memory element for storing a unit of binary information, comprising the magnetic latch of claim [[9]] 14.

14. (previously presented) A magnetic latch for detecting an external magnetic field comprising the field effect transistor of claim 1, further comprising a reset switch connected between said first supplemental gate and said second supplemental gate, to short said first supplemental gate and said second supplemental gates to reset said latch.